Low Cost, 300 MHz
Voltage Feedback Amplifiers

AD8055/AD8056

FEATURES
Low Cost Single (AD8055) and Dual (AD8056)
Easy to Use Voltage Feedback Architecture
High Speed
　　300 MHz, –3 dB Bandwidth (G = +1)
　　1400 V/μs Slew Rate
　　20 ns Settling to 0.1%
　　Low Distortion: –72 dBc @ 10 MHz
　　Low Noise: 6 nV/$\sqrt{Hz}$
　　Low DC Errors: 5 mV Max V_{OS}, 1.2 μA Max I_B
Small Packaging
　　AD8055 Available in SOT-23-5
　　AD8056 Available in 8-Lead microSOIC
Excellent Video Specifications (R_L = 150 Ω, G = +2)
　　Gain Flatness 0.1 dB to 40 MHz
　　0.01% Differential Gain Error
　　0.02° Differential Phase Error
　　Drives Four Video Loads (37.5 Ω) with 0.02% and
　　　0.1° Differential Gain and Differential Phase
Low Power, ±5 V Supplies
　　5 mA Typ/Amplifier Power Supply Current
High Output Drive Current: Over 60 mA

APPLICATIONS
Imaging
Photodiode Preamp
Video Line Driver
Differential Line Driver
Professional Cameras
Video Switchers
**Special Effects**
A-to-D Driver
Active Filters

PRODUCT DESCRIPTION
The AD8055 (single) and AD8056 (dual) voltage feedback amplifiers offer bandwidth and slew rate typically found in current feedback amplifiers. Additionally, these amplifiers are easy to use and available at a very low cost.

Despite their low cost, the AD8055 and AD8056 provide excellent overall performance. For video applications, their differential gain and phase error are 0.01% and 0.02° into a 150 Ω load, and 0.02% and 0.1° while driving four video loads (37.5 Ω). Their 0.1 dB flatness out to 40 MHz, wide bandwidth out to 300 MHz, along with 1400 V/μs slew rate and 20 ns settling time, make them useful for a variety of high-speed applications.
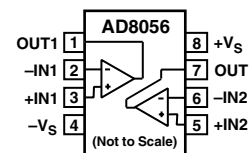
FUNCTIONAL BLOCK DIAGRAMS

N-8 and R-8
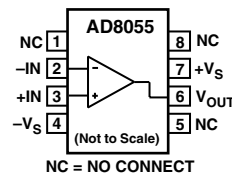
SOT-23-5 (RT)
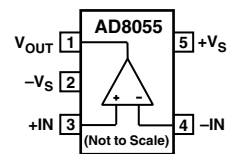
N-8, R-8, microSOIC (RM)

The AD8055 and AD8056 require only 5 mA typ/amplifier of supply current and operate on dual ±5 V or single +12 V power supply, while being capable of delivering over 60 mA of load current. All this is offered in a small 8-lead plastic DIP, 8-lead SOIC packages, 5-lead SOT-23-5 package (AD8055) and an 8-lead microSOIC package (AD8056). These features make the AD8055/AD8056 ideal for portable and battery powered applications where size and power are critical. These amplifiers are available in the industrial temperature range of –40°C to +85°C.

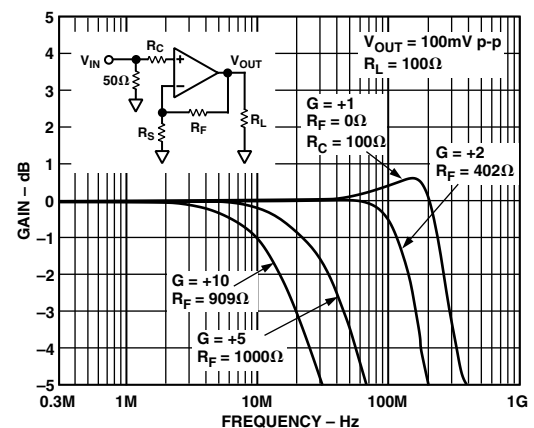*Figure 1. Frequency Response*

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AD8055/AD8056–SPECIFICATIONS (@ T_A = 25°C, V_S = ±5 V, R_F = 402 Ω, R_L = 100 Ω, Gain = +2, unless otherwise noted)

Model	Conditions	AD8055A/AD8056A Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +1, V_O = 0.1 V p-p	220	300		MHz
	G = +1, V_O = 2 V p-p	125	150		MHz
	G = +2, V_O = 0.1 V p-p	120	160		MHz
	G = +2, V_O = 2 V p-p	125	150		MHz
Bandwidth for 0.1 dB Flatness	V_O = 100 mV p-p	25	40		MHz
Slew Rate	G = +1, V_O = 4 V Step	1000	1400		V/μs
	G = +2, V_O = 4 V Step	750	840		V/μs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		20		ns
Rise and Fall Time, 10% to 90%	G = +1, V_O = 0.5 V Step		2		ns
	G = +1, V_O = 4 V Step		2.7		ns
	G = +2, V_O = 0.5 V Step		2.8		ns
	G = +2, V_O = 4 V Step		4		ns
NOISE/HARMONIC PERFORMANCE					
Total Harmonic Distortion	f_C = 10 MHz, V_O = 2 V p-p, R_L = 1 kΩ		–72		dBc
	f_C = 20 MHz, V_O = 2 V p-p, R_L = 1 kΩ		–57		dBc
Crosstalk, Output to Output (AD8056)	f = 5 MHz, G = +2		–60		dB
Input Voltage Noise	f = 100 kHz		6		nV/√Hz
Input Current Noise	f = 100 kHz		1		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.01		%
	R_L = 37.5 Ω		0.02		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.02		Degree
	R_L = 37.5 Ω		0.1		Degree
DC PERFORMANCE					
Input Offset Voltage			3	5	mV
	T_{MIN}–T_{MAX}			10	mV
Offset Drift			6		μV/°C
Input Bias Current			0.4	1.2	μA
	T_{MIN}–T_{MAX}		1		μA
Open Loop Gain	V_O = ±2.5 V	66	71		dB
	T_{MIN}–T_{MAX}	64			dB
INPUT CHARACTERISTICS					
Input Resistance			10		MΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range			3.2		±V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V		82		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 150 Ω	2.9	3.1		±V
Output Current[1]	V_O = ±2.0 V	55	60		mA
Short Circuit Current[1]			110		mA
POWER SUPPLY					
Operating Range		±4.0	±5.0	±6.0	V
Quiescent Current	AD8055		5.4	6.5	mA
	T_{MIN}–T_{MAX}			7.3	mA
	AD8056		10	12	mA
	T_{MIN}–T_{MAX}			13.3	mA
Power Supply Rejection Ratio	+V_S = +5 V to +6 V, –V_S = –5 V	66	72		dB
	–V_S = –5 V to –6 V, +V_S = +5 V	69	86		dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

NOTES
[1]Output current is limited by the maximum power dissipation in the package. See the power derating curves.

Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . 13.2 V

Internal Power Dissipation[2]

   Plastic DIP Package (N) . . . . 1.3 W

   Small Outline Package (R) . . . . 0.8 W

   SOT-23-5 Package (RT) . . . . 0.5 W

   microSOIC Package (RM) . . . . 0.6 W

Input Voltage (Common Mode) . . . . $\pm V_S$

Differential Input Voltage . . . . ± 2.5 V

Output Short Circuit Duration

   . . . . Observe Power Derating Curves

Storage Temperature Range N, R . . . . –65°C to +125°C

Operating Temperature Range (A Grade) . . –40°C to +85°C

Lead Temperature Range (Soldering 10 sec) . . . . 300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent
damage to the device. This is a stress rating only; functional operation of the device at
these or any other conditions above those indicated in the operational section of this
specification is not implied. Exposure to absolute maximum rating conditions for
extended periods may affect device reliability.

[2]Specification is for device in free air:
  8-Lead Plastic DIP Package: $\theta_{JA} = 90°C/W$
  8-Lead SOIC Package: $\theta_{JA} = 155°C/W$
  5-Lead SOT-23-5 Package: $\theta_{JA} = 240°C/W$
  8-Lead microSOIC Package: $\theta_{JA} = 200°C/W$

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8055/
AD8056 is limited by the associated rise in junction temperature.
The maximum safe junction temperature for plastic encapsulated
devices is determined by the glass transition temperature of the

plastic, approximately 150°C. Exceeding this limit temporarily
may cause a shift in parametric performance due to a change in
the stresses exerted on the die by the package. Exceeding a
junction temperature of 175°C for an extended period can result
in device failure. www.trimmer.ru

While the AD8055/AD8056 are internally short circuit protected,
this may not be sufficient to guarantee that the maximum junction
temperature (150°C) is not exceeded under all conditions. To
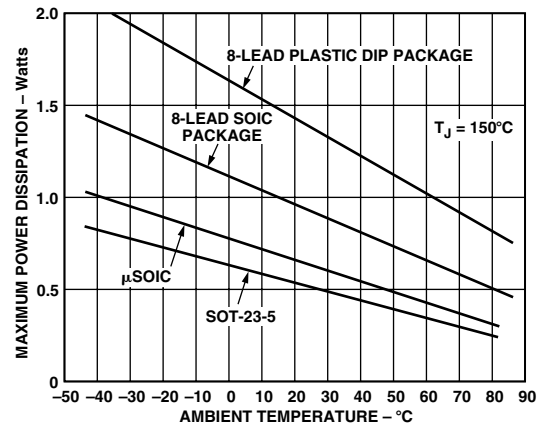ensure proper operation, it is necessary to observe the maximum
power derating curves.

Figure 2. Plot of Maximum Power Dissipation vs.
Temperature for AD8055/AD8056

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding Code
AD8055AN	–40°C to +85°C	Plastic DIP	N-8	
AD8055AR	–40°C to +85°C	Small Outline Package (SOIC)	SO-8	
AD8055AR-REEL	–40°C to +85°C	13" Tape and Reel	SO-8	
AD8055AR-REEL7	–40°C to +85°C	7" Tape and Reel	SO-8	
AD8055ART-REEL	–40°C to +85°C	13" Tape and Reel	RT-5	H3A
AD8055ART-REEL7	–40°C to +85°C	7" Tape and Reel	RT-5	H3A
AD8056AN	–40°C to +85°C	Plastic DIP	N-8	
AD8056AR	–40°C to +85°C	Small Outline Package (SOIC)	SO-8	
AD8056AR-REEL	–40°C to +85°C	13" Tape and Reel	SO-8	
AD8056AR-REEL7	–40°C to +85°C	7" Tape and Reel	SO-8	
AD8056ARM	–40°C to +85°C	microSOIC	RM-8	H5A
AD8056ARM-REEL	–40°C to +85°C	13" Tape and Reel	RM-8	H5A
AD8056ARM-REEL7	–40°C to +85°C	7" Tape and Reel	RM-8	H5A

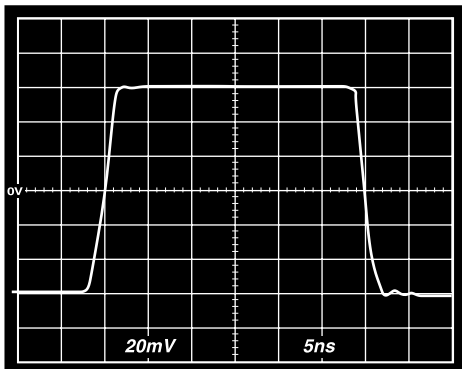# AD8055/AD8056–Typical Performance Characteristics
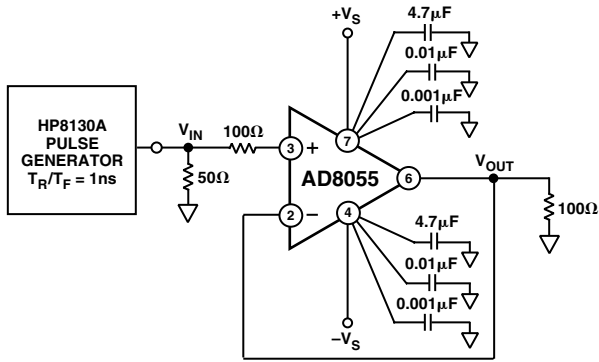
TPC 1. Test Circuit, G = +1, R_L = 100 Ω
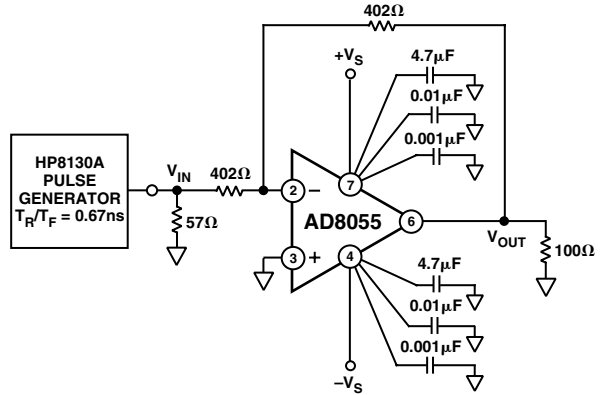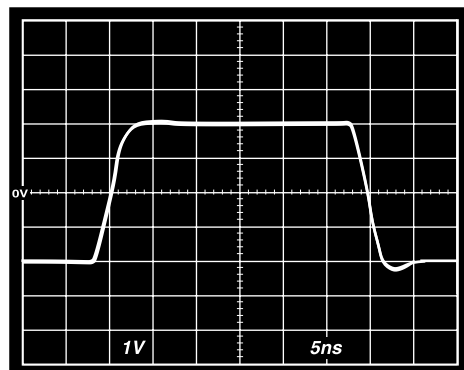

TPC 4. Test Circuit, G = –1, R_L = 100 Ω

TPC 2. Small Step Response, G = +1
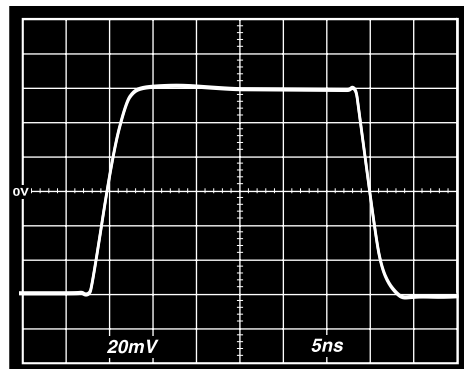
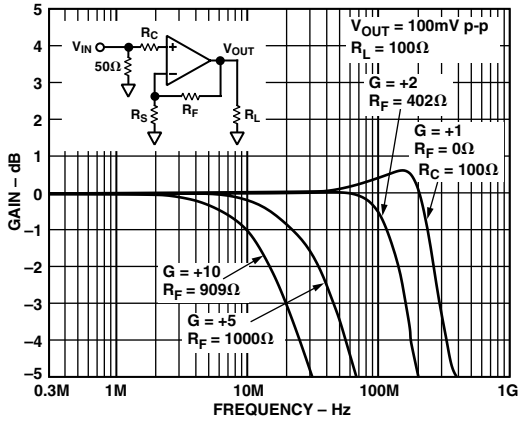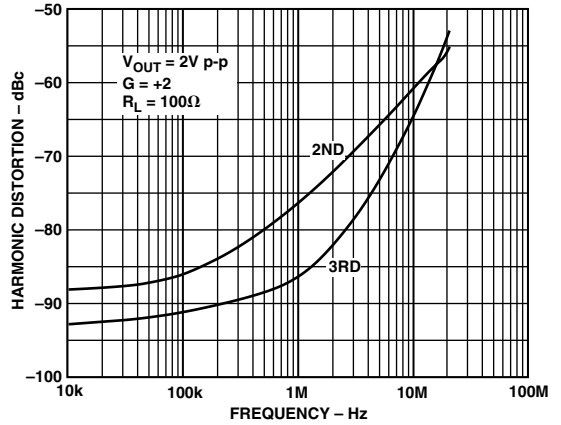TPC 5. Small Step Response, G = –1
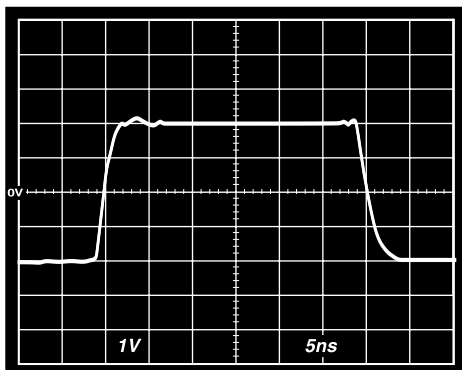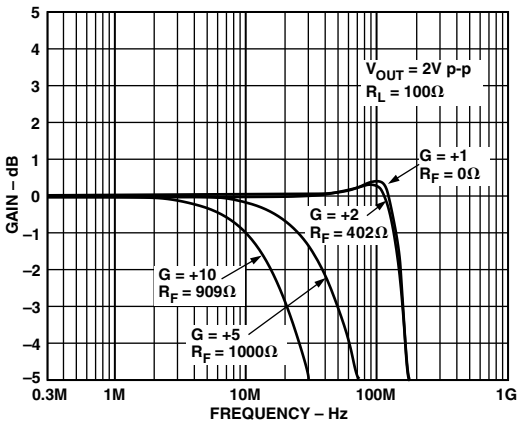

TPC 3. Large Step Response, G = +1
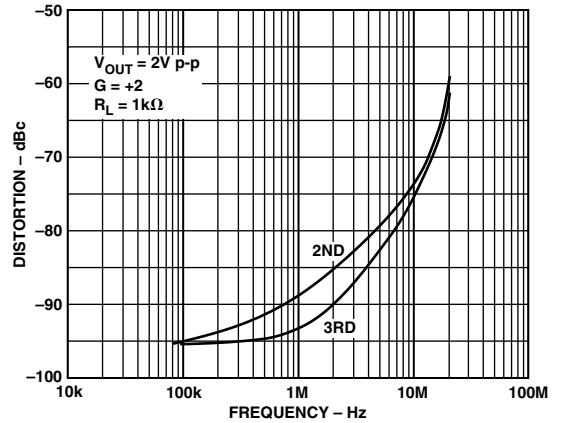

TPC 6. Large Step Response, G = –1

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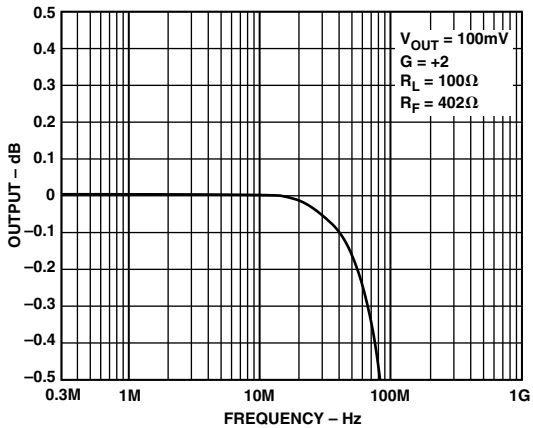TPC 7. Small Signal Frequency Response,
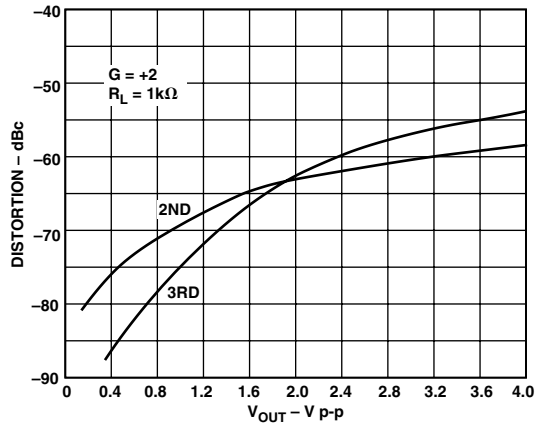G = +1, G = +2, G = +5, G = +10

TPC 10. Distortion vs. Frequency

TPC 8. Large Signal Frequency Response,
G = +1, G = +2, G = +5, G = +10

TPC 11. Distortion vs. Frequency

TPC 9. 0.1 dB Flatness

TPC 12. Distortion vs. V_{OUT} @ 20 MHz

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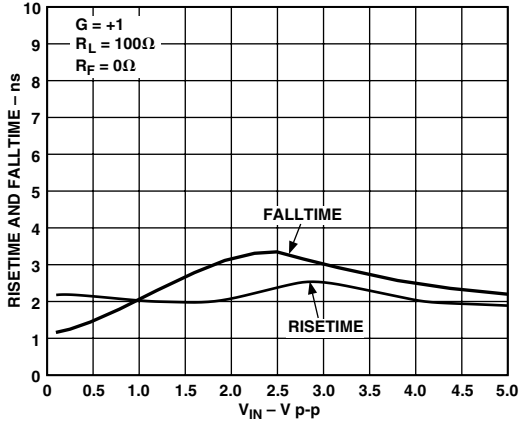
TPC 13. Risetime and Falltime vs. V_{IN}
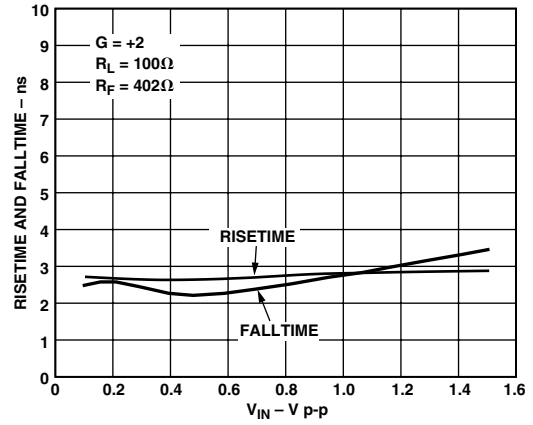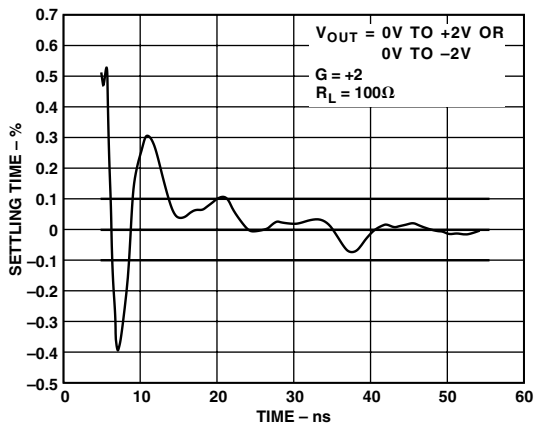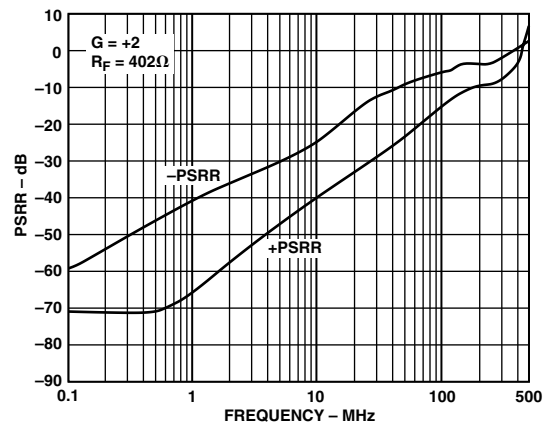

TPC 14. Risetime and Falltime vs. V_{IN}

TPC 15. Settling Time

TPC 16. Risetime and Falltime vs. V_{IN}
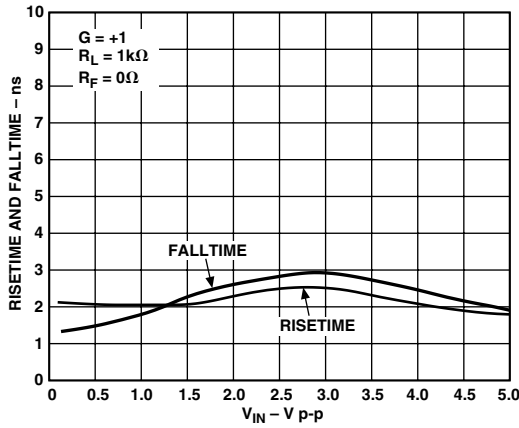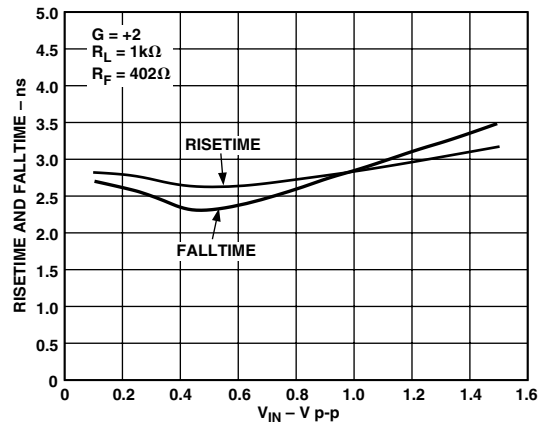
TPC 17. Risetime and Falltime vs. V_{IN}
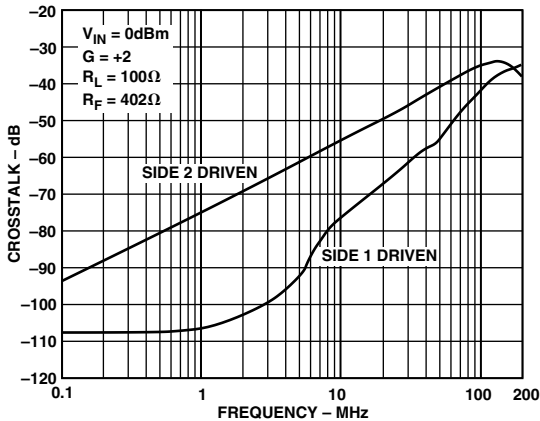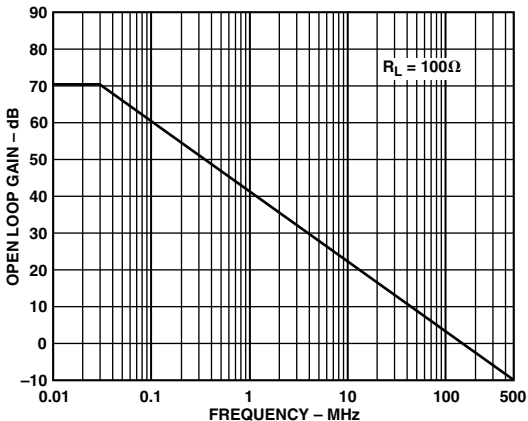

TPC 18. PSRR vs. Frequency
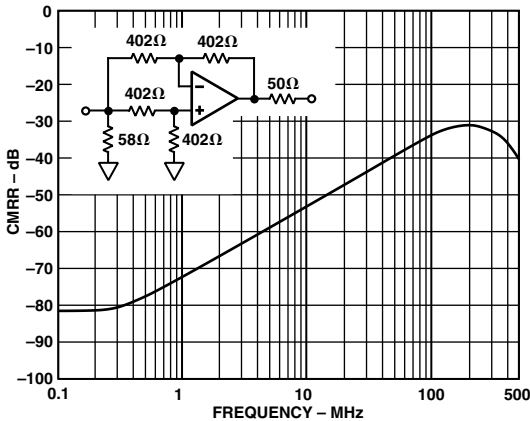
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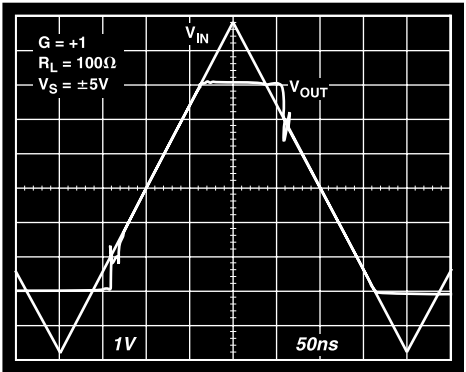
TPC 19. Overload Recovery
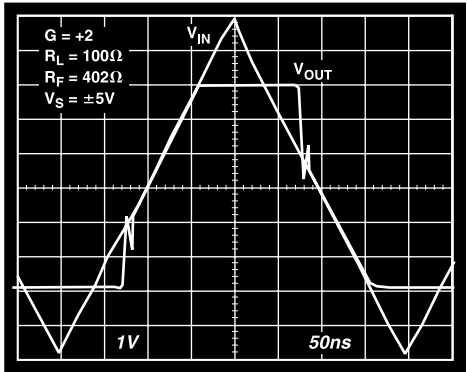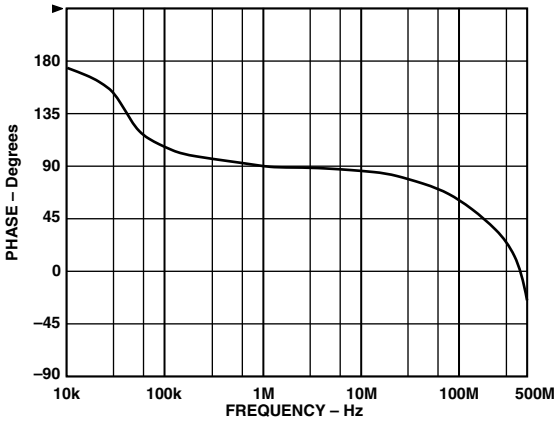

TPC 22. Overload Recovery

TPC 20. Crosstalk (Output-to-Output) vs. Frequency

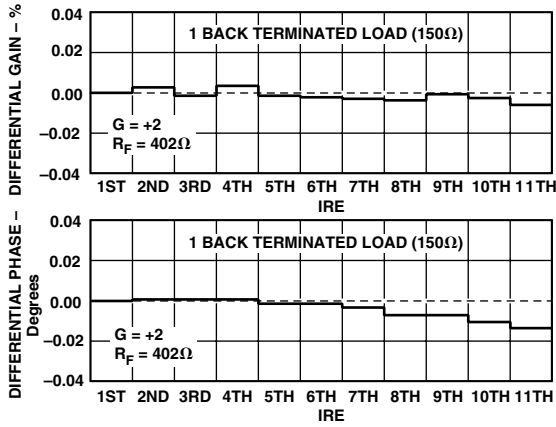TPC 23. Open Loop Gain vs. Frequency

TPC 21. CMRR vs. Frequency
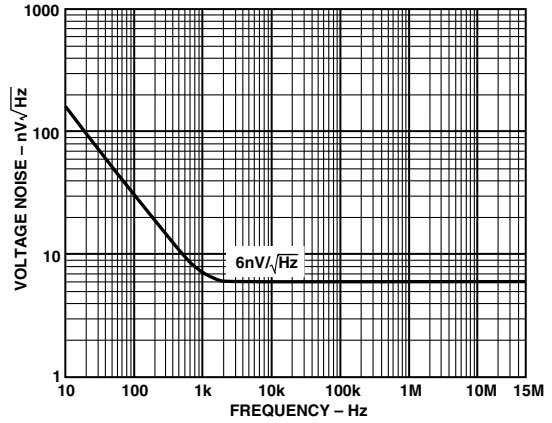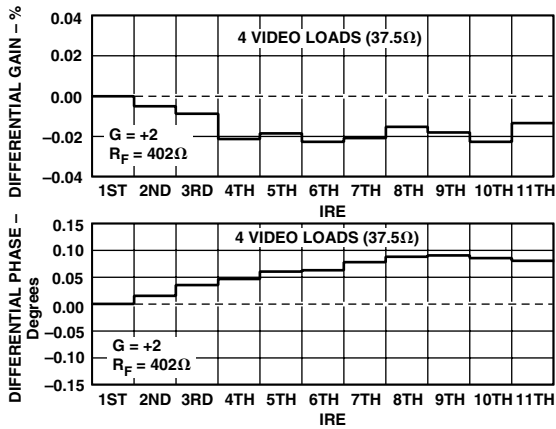

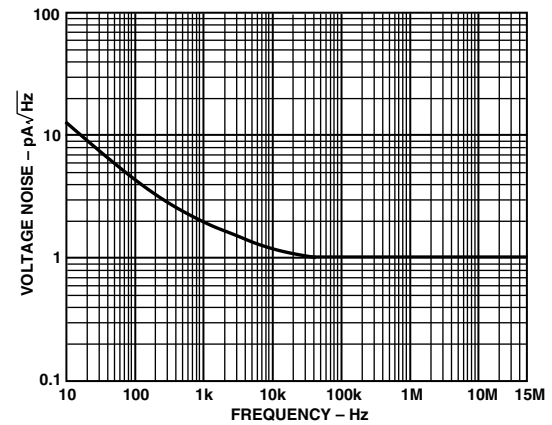TPC 24. Phase vs. Frequency

AD8055/AD8056

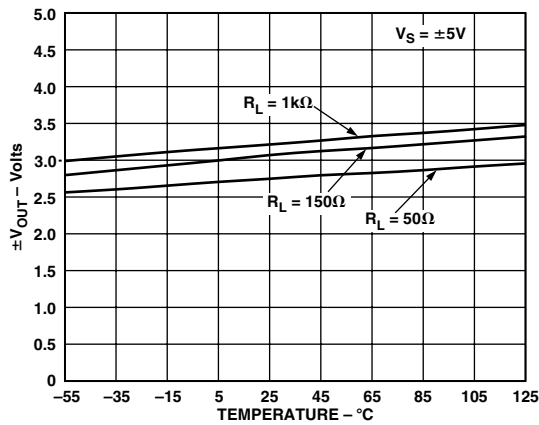TPC 25. Differential Gain and Differential Phase

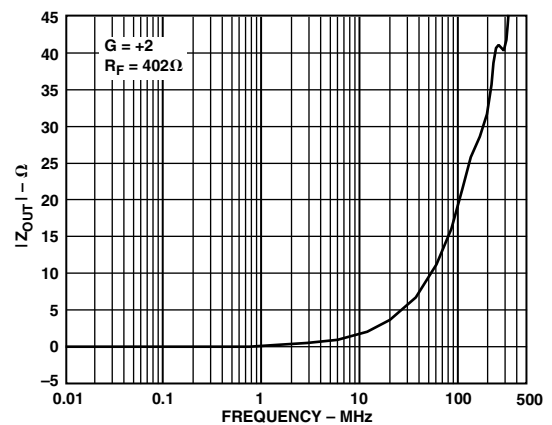
TPC 28. Voltage Noise vs. Frequency

TPC 26. Differential Gain and Differential Phase

TPC 29. Current Noise vs. Frequency

TPC 27. Output Swing vs. Temperature

TPC 30. Output Impedance vs. Frequency

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APPLICATIONS

Four-Line Video Driver

The AD8055 is a useful low cost circuit for driving up to four video lines. For such an application, the amplifier is configured for a noninverting gain of 2 as shown in Figure 3. The input video source is terminated in 75 Ω and applied to the high impedance noninverting input.

Each output cable is connected to the op amp output via a 75 Ω series back termination resistor for proper cable termination. The terminating resistors at the other ends of the lines will divide the output signal by two, which is compensated for by the gain-of-two of the op amp stage.

For a single load, the differential gain error of this circuit was measured to be 0.01%, with a differential phase error of 0.02 degrees. The two load measurements were 0.02% and 0.03 degrees, respectively. For four loads, the differential gain error is 0.02%, while the differential phase increases to 0.1 degrees.
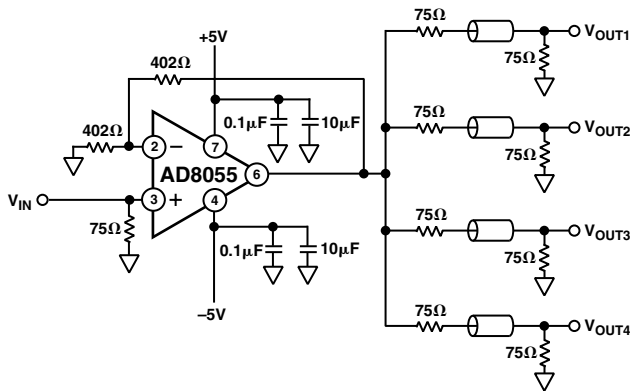

Figure 3. Four-Line Video Driver

Single-Ended to Differential Line Driver

Creating differential signals from single-ended signals is required for driving balanced, twisted pair cables, differential input A/D converters and other applications that require differential signals. This is sometimes accomplished by using an inverting and a non-inverting amplifier stage to create the complementary signals.

The circuit shown in Figure 4 shows how an AD8056 can be used to make a single-ended to differential converter that offers some advantages over the architecture mentioned above. Each op amp is configured for unity gain by the feedback resistors from the outputs to the inverting inputs. In addition, each output drives the opposite op amp with a gain of –1 by means of the crossed resistors. The result of this is that the outputs are complementary and there is high gain in the overall configuration.

Feedback techniques similar to a conventional op amp are used to control the gain of the circuit. From the noninverting input of Amp 1 to the output of Amp 2, is an inverting gain. Between these points a feedback resistor can be used to close the loop. As in the case of a conventional op amp inverting gain stage, an input resistor is added to vary the gain.

The gain of this circuit from the input to Amp 1 output is R_F/R_I, while the gain to the output of Amp 2 is $–R_F/R_I$. The circuit thus creates a balanced differential output signal from a single-ended input. The advantage of this circuit is that the gain can be changed by changing a single resistor and still maintain the balanced differential outputs.
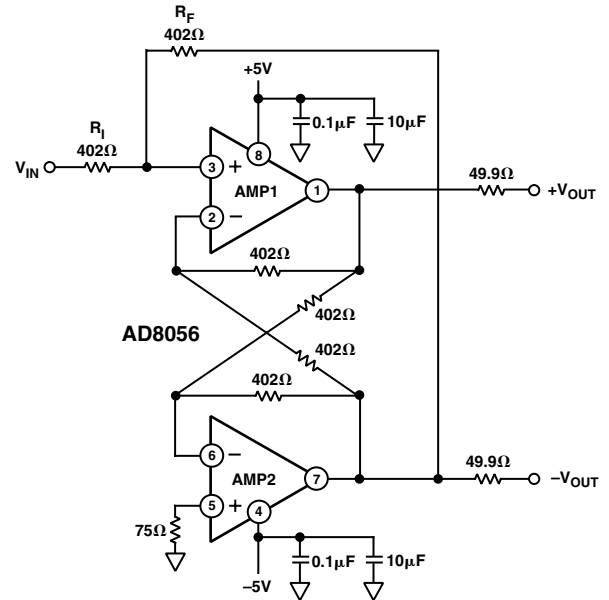

Figure 4. Single-Ended to Differential Line Driver

Low Noise, Low Power Preamp

The AD8055 makes a good, low cost, low noise, low power preamp. A gain of 10 preamp can be made with a feedback resistor of 909 Ω and a gain resistor of 100 Ω as shown in Figure 5. The circuit has a –3 dB bandwidth of 20 MHz.
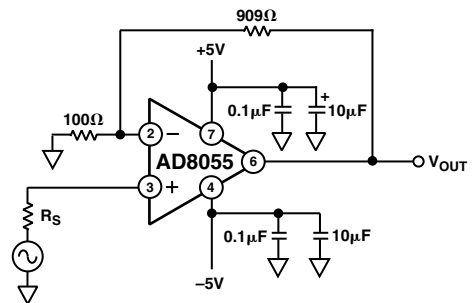

Figure 5. Low Noise, Low Power Preamp with G = +10 and BW = 20 MHz

With a low source resistance (<approximately 100 Ω), the major contributors to the input referred noise of this circuit are the input voltage noise of the amplifier and the noise of the 100 Ω resistor. These are 6 nV/$\sqrt{Hz}$ and 1.2 nV/$\sqrt{Hz}$, respectively. These values yield a total input referred noise of 6.1 nV/$\sqrt{Hz}$.

AD8055/AD8056

Power Dissipation Limits

With a 10 V supply (total $V_{CC} - V_{EE}$), the quiescent power dissipation of the AD8055 in the SOT-23-5 package is 65 mW, while the quiescent power dissipation of the AD8056 in the microSOIC is 120 mW. This translates into a 15.6°C rise above the ambient for the SOT-23-5 package and a 24°C rise for the microSOIC package.

The power dissipated under heavy load conditions is approximately equal to the supply voltage minus the output voltage, times the load current, plus the quiescent power computed above. This total power dissipation is then multiplied by the thermal resistance of the package to find the temperature rise, above ambient, of the part. The junction temperature should be kept below 150°C.

The AD8055 in the SOT-23-5 package can dissipate 270 mW while the AD8056 in the microSOIC package can dissipate 325 mW (at 85°C ambient) without exceeding the maximum die temperature. In the case of the AD8056, this is greater than 1.5 V rms into 50 Ω, enough to accommodate a 4 V p-p sine-wave signal on both outputs simultaneously. But since each output of the AD8055 or AD8056 is capable of supplying as much as 110 mA into a short circuit, a continuous short circuit condition will exceed the maximum safe junction temperature.

Resistor Selection

The following table is provided as a guide to resistor selection for maintaining gain flatness vs. frequency for various values of gain.

Gain	R_F (Ω)	R_I (Ω)	−3 dB Bandwidth (MHz)
+1	0	—	300
+2	402	402	160
+5	1k	249	45
+10	909	100	20

Driving Capacitive Loads

When driving a capacitive load, most op amps will exhibit peaking in the frequency response just before the frequency rolls off. Figure 6 shows the responses for an AD8056 running at a gain of +2, with a 100 Ω load that is shunted by various values of capacitance. It can be seen that under these conditions, the part is still stable with capacitive loads of up to 30 pF.
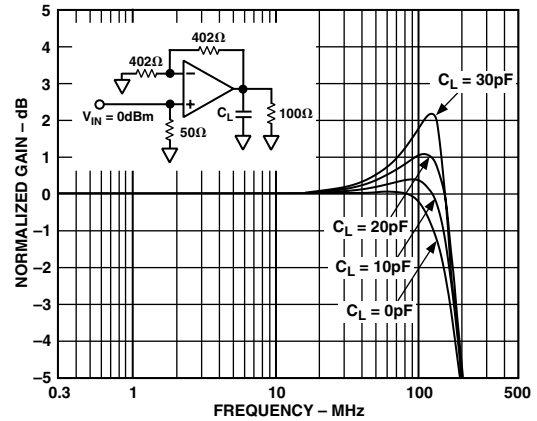

Figure 6. Capacitive Load Drive

In general, to minimize peaking or to ensure the stability for larger values of capacitive loads, a small series resistor, R_S, can be added between the op amp output and the capacitor, C_L. For the setup depicted in Figure 7, the relationship between R_S and C_L was empirically derived and is shown in Figure 8. R_S was chosen to produce less than 1 dB of peaking in the frequency response. Note also that after a sharp rise R_S quickly settles to about 25 Ω.
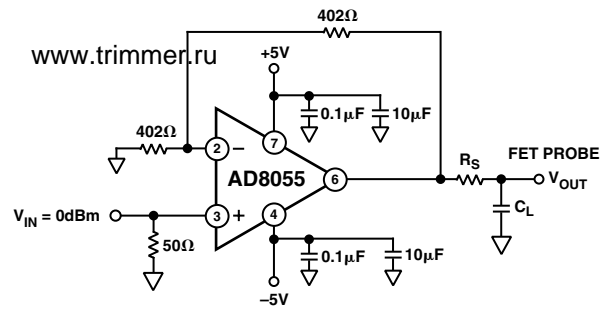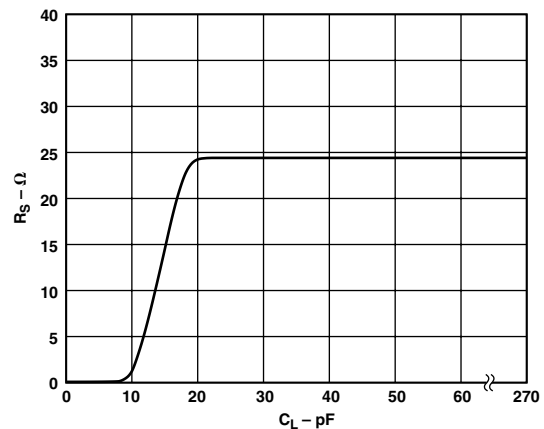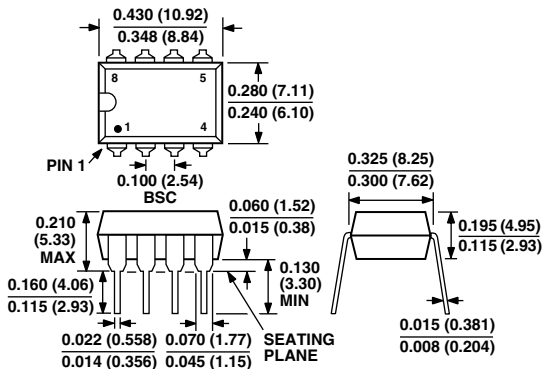

Figure 7. Setup for R_S vs. C_L

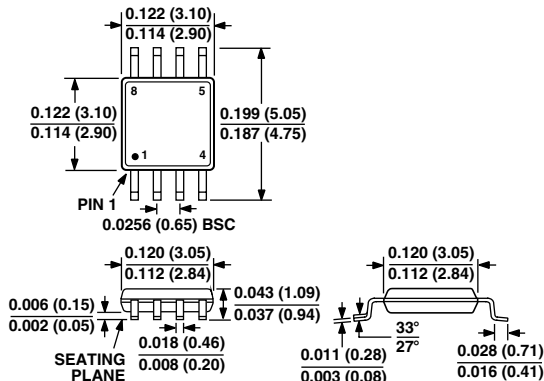*Figure 8. R_S vs. C_L*

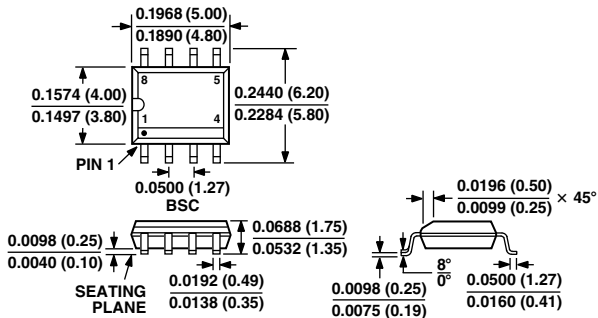## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

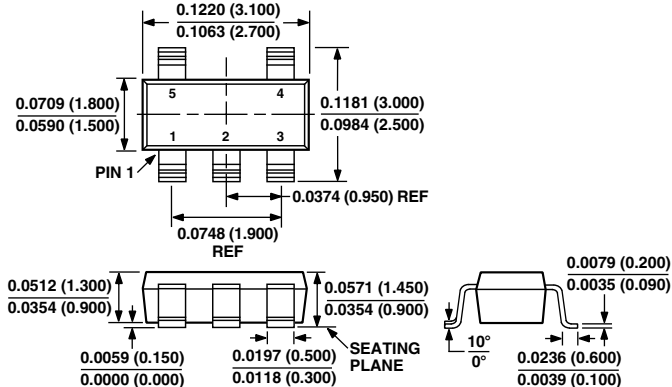**8-Lead Plastic DIP**
(N-8)

8-Lead microSOIC Package
(RM-8)

8-Lead Small Outline SOIC
(R-8)

5-Lead Plastic Surface Mount
(RT-5)

AD8055/AD8056

Revision History