SPECIFICATION

for

MRD531B-LQ

Triple Channel F2F Decoder IC

Revision A
05 Jun. 2002

Uniform Industrial Corp.

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Triple Channel F2F Decoder IC

1. DESCRIPTION

The MRD531B-LQ is a 0.8um CMOS integrated circuit for the purpose of recovering F2F encoded data received from a magnetic head.

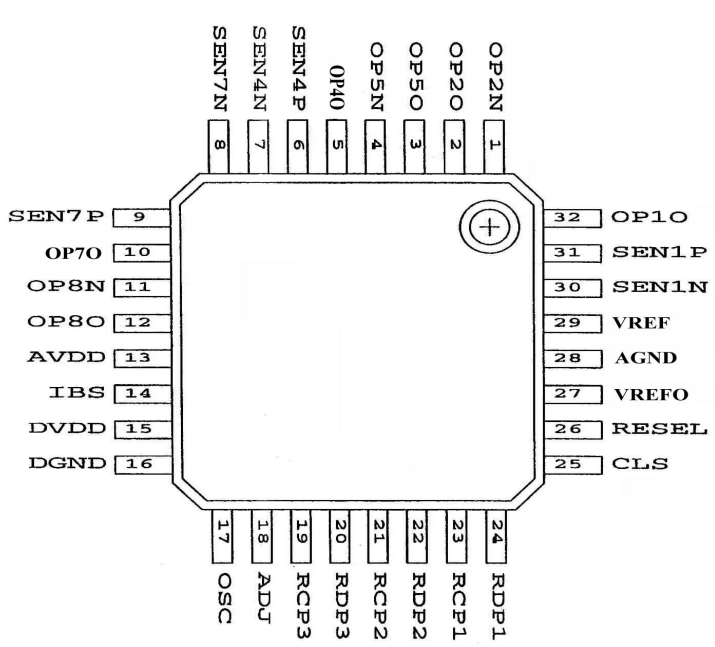
2. FEATURES

- Integrated Amplification Circuit for magnetic head signal.
- Both output polarities supported.
- Adjustable read data output clock pulse width.
- Triple channel and support for 75/210bpi recording density.
- Magnetic head data input frequency range from 300 bit/sec to 12600 bit/sec.
- Power-down stand-by mode to reduce current consumption.
- Provide the option of 8 or 11 leading bits ignored
- Enhanced noise filter
- Automatic offset voltage cancellation circuit for amplifiers
- Advanced algorithm to effectively read poor condition cards as well as high jitter cards

3. APPLICATIONS

- Magnetic stripe card reader
- POS Keyboard

PIN Configuration (Top View)



LQFP-32 10mmx10mm

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4. PIN DESCRIPTION

1	OP2N	Inverting input of second stage amplifier for channel 1
2	OP2O	Output of second stage amplifier for channel 1
3	OP5O	Output of second stage amplifier for channel 2
4	OP5N	Inverting input of second stage amplifier for channel 2
5	OP4O	Output of first stage amplifier for channel 2
6	SEN4P	Non-inverting input of first stage amplifier for channel 2
7	SEN4N	Inverting input of first stage amplifier for channel 2
8	SEN7N	Inverting input of first stage amplifier for channel 3
9	SEN7P	Non-inverting input of first stage amplifier for channel 3
10	OP7O	Output of first stage amplifier for channel 3
11	OP8N	Inverting input of second stage amplifier for channel 3
12	OP8O	Output of second stage amplifier for channel 3
13	AVDD	Positive power supply, Analog VDD
14	IBS	Leading Ignore Bit Select
15	DVDD	Positive power supply, Digital VDD
16	DGND	Substrate connected to digital ground
17	OSC	RC oscillator input
18	ADJ	RCP pulse width adjust
19	RCP3	Received clock pulse for channel 3
20	RDP3	Received data pulse for channel 3
21	RCP2	Received clock pulse for channel 2
22	RDP2	Received data pulse for channel 2
23	RCP1	Received clock pulse for channel 1
24	RDP1	Received data pulse for channel 1
25	CLS	Card loading signal output
26	RESEL	Reset and select for RDP output polarity
27	VREFO	Buffered reference voltage for Op-amp bias
28	AGND	Analog Ground
29	VREF	Reference voltage for Op-Amp bias
30	SEN1N	Inverting input of first stage amplifier for channel 1
31	SEN1P	Non-inverting input of first stage amplifier for channel 1
32	OP1O	Output of first stage amplifier for channel 1

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5. FUNCTION DESCRIPTION

The magnetic card data signal received from magnetic head is first fed into the first stage operational amplifier, which provides a voltage gain of 16 or 11 according to the VDD supply voltage. The high frequency noise is filtered through the second stage operational amplifier. The second stage operational amplifier not only performs the noise filtering but also decides where the signal peaks occur. Its output with voltage clamp is sent to Waveform Shaping circuit to generate the logic level F2F format data. Once receiving the F2F signals, the decoder circuit ignores 11 (or 8) leading bits and determines the reference bit length by calculating the preceding bits.

If the F2F signal toggles before 75% of the reference bit length, it would be identified as bit 1, and the next F2F signal toggle will be identified as the beginning of next data bit. If the F2F signal toggles after 75% of the reference bit length, it would be identified as bit 0, and the current F2F signal toggle will be identified as the beginning of next bit.

Following ignored bits, Card Load Signal (CLS) will be pulled low and keep low as long as F2F signal toggle continuously. When F2F signal no longer toggles for a time period of 30720 FOSC clocks (about 7.7ms if FOSC=4MHz), the CLS will go high, and enter power-down stand-by mode.

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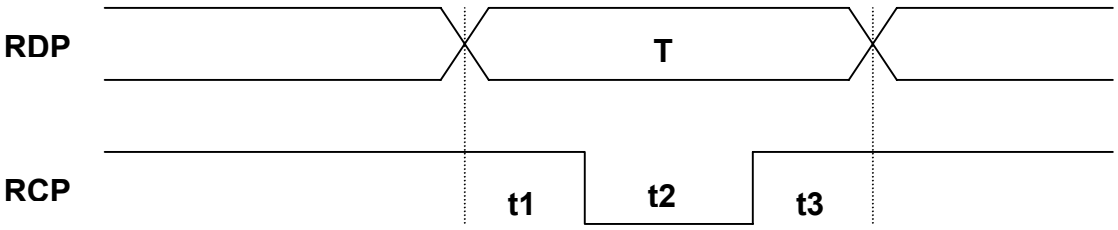
The timing relationship of RCP and RDP output signals is shown as below:



T = t1+t2+t3: data bit length

t1 = 7 * OSC_clock

t2 = 20 * OSC_clock + 16 * ADJ_clock

t3 >= 2 * OSC_clock

t2 <= 272 * OSC_clock

OSC_clock, ADJ_clock are determined by external R/C components, which are connected to OSC and ADJ pins respectively. The relation between Radj and t2 is shown in Table-1 with external 18K ohm and 22 pf connected to OSC pin.

RESEL pin provides two functions, the chip reset and the selection of data polarity for RDP output. The RDP output would be positive polarity if RESEL pin stays at logic high level. It would be changed to inverting polarity if RESET stays at logic low level. A logic level change either from High to Low or Low to High on RESEL pin will reset the whole chip and cause it to enter power down stand-by mode.

VREF is designed to generate the DC bias voltage for operational amplifiers to operate. The voltage of VREF could be roughly expressed as follows:

$$VREF=(VDD-1.3)/2$$

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The first stage operational amplifier is used to pick up the small signal from magnetic head and amplifies the signal with appropriate voltage gain, which varies with the VDD supply voltage and card swiping speed. When VDD is higher than 4 volts, the voltage gain of the first stage op-amp for normal swipe speed is internally set to 16. When VDD is below than 4 volts, the voltage gain for normal swipe speed will be changed to 11.

The band-pass filtering and peak-detection is implemented by the external R/C components, which are connected between first stage amplifier and second stage amplifier.

In addition to the band-pass filter, a built-in active filter next to the second stage op-amp and the waveform shaping circuit effectively eliminates the abnormal signal reversal between adjacent F2F signals.

The clamp voltage of the second stage op-amp varies with the VDD supply voltage. It is set at approximate VREF+/-0.6 volts if VDD equals 5 volts, and changed to approximate VREF+/- 0.4 volts if VDD equals 3.3 volts.

6. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
VCC	Supply voltage	VDD	-0.5 to +7.0	V
Vin	Input voltage		-0.5 to Vcc +0.5	V
Io	Output current	RCP, RDP, CLS	-10 to +10	mA
Vid	Differential input voltage	SENXP~SENXN	-1.0 to +1.0	V
Topr	Operating temperature		-10 to +70	°C
Tstg	Storage temperature		-50 to +140	°C

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7. RECOMMENDED OPERATING CONDITIONS

There are two operating conditions, VCC=5.0V and VCC=3.3V

a. VCC=5.0V

Symbol	Parameter	Conditions	Ratings			Unit
			Min.	Typ.	Max.	
VCC	Supply Voltage	VDD	4.5	5	5.5	V
VIH	Input High Voltage	RESEL	VCC-0.5			V
VIL	Input Low Voltage	RESEL			0.5	V
IOH	Output High Source Current at VOH=VCC-0.4V	RCP, RDP	1.0	1.5	2.0	mA
IOH	Output High Source Current at VOH=VCC-0.4V	CLS	4.0	8.0	12.0	uA
IOL	Output Low Sink Current at VOL=0.4V	RCP, RDP, CLS	2.5	3.5	5.0	mA
FOSC	Oscillation Frequency	Rosc=18KHz, Cosc=22pF		4.0		MHz
IOPR	Operation Current	No Load	1.6	1.9	2.3	mA
ISBY	Standby Current	No Load	1.2	1.35	1.65	mA

TABLE-1a TYPICAL RELATION OF Radj and RCP PULSE WIDTH

Condition: Rosc=18Kohm, Cosc=22pF, VDD=5.0V

Radj(Ohm)	15K	20K	30K	50K	100K	200K	330K	510K	680K	1M~2M
t2 (us) Typ.	7	7.3	8.2	9.5	13.6	21.5	32	46	60	68

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b. VCC=3.3V

Symbol	Parameter	Conditions	Ratings			Unit
			Min.	Typ.	Max.	
VCC	Supply Voltage	VDD	3.0	3.3	3.6	V
VIH	Input High Voltage	RESEL	VCC-0.5			V
VIL	Input Low Voltage	RESEL			0.5	V
IOH	Output High Source Current at VOH=VCC-0.4V	RCP, RDP	0.3	0.6	1.0	mA
IOH	Output High Source Current at VOH=VCC-0.4V	CLS	2.0	4.0	6.0	uA
IOL	Output Low Sink Current at VOL=0.4V	RCP, RDP, CLS	0.8	1.5	2.5	mA
FOSC	Oscillation Frequency	Rosc=18KHz, Cosc=22pF		4.0		MHz
IOPR	Operation Current	No Load	0.9	1.1	1.3	mA
ISBY	Standby Current	No Load	0.75	0.85	0.95	mA

TABLE-1b TYPICAL RELATION OF Radj and RCP PULSE WIDTH

Condition: Rosc=18Kohm, Cosc=22pF, VDD=3.3V

Radj(Ohm)	15K	20K	30K	50K	100K	200K	330K	510K	680K	1M~2M
t2 (us) Typ.	7.2	7.5	8.2	9.4	13.1	20.3	29	43	55	68

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8. ELECTRONIC CHARACTERISTICS OF OP-AMP

a. VCC=5.0V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vref	Reference Voltage	No external R	1.6	1.8	2.0	V
Vio	Offset Voltage		--	3	10	mV
Voh	Output Voltage	OP1, OP4, OP7	--	--	3.5	V
VoL	Output Voltage	OP1, OP4, OP7	0.05	--	--	V
Voh	Output Voltage	OP2, OP5, OP8	Vref+0.4	Vref+0.6	Vref+0.8	V
VoL	Output Voltage	OP2, OP5, OP8	Vref-0.8	Vref-0.6	Vref-0.4	V
Avd	Small Signal Differential Voltage Gain	OP1, OP4, OP7 Vid=10~60mV @15KHz Sine wave	14	16	18	V/V
Ri	Input Resistance	OP1, OP4, OP7	6	8	12	Kohm
Fvid	Output Frequency	OP1, OP4, OP7 Vid=5~80mVp-p	300	--	15K	Hz
GB	Gain-Bandwidth	OP1, OP4, OP7 OP2, OP5, OP8	1	--	2	MHz
Vid	Differential Input Voltage	SENXP~SENXN	5	--	80	mV

b. VCC=3.3V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vref	Reference Voltage	No external R	0.85	1.0	1.15	V
Vio	Offset Voltage		--	3	10	mV
Voh	Output Voltage	OP1, OP4, OP7	--	--	2.0	V
VoL	Output Voltage	OP1, OP4, OP7	0.05	--	--	V
Voh	Output Voltage	OP2, OP5, OP8	Vref+0.3	Vref+0.4	Vref+0.5	V
VoL	Output Voltage	OP2, OP5, OP8	Vref-0.5	Vref-0.4	Vref-0.3	V
Avd	Small Signal Differential Voltage Gain	OP1, OP4, OP7 Vid=10~60mV @15KHz Sine wave	9.5	11	12.5	V/V
Ri	Input Resistance	OP1, OP4, OP7	6	8	12	Kohm
Fvid	Output Frequency	OP1, OP4, OP7 Vid=5~80mVp-p	300	--	15K	Hz
GB	Gain-Bandwidth	OP1, OP4, OP7 OP2, OP5, OP8	1	--	2	MHz
Vid	Differential Input Voltage	SENXP~SENXN	5	--	80	mV

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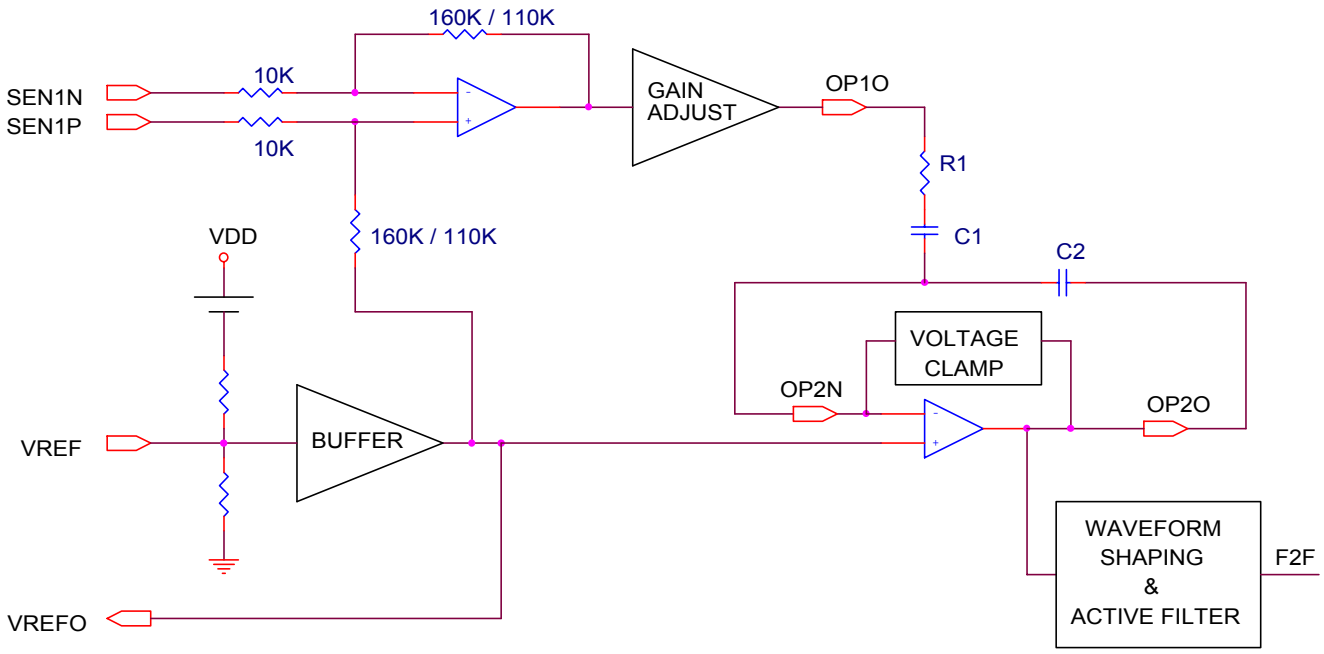
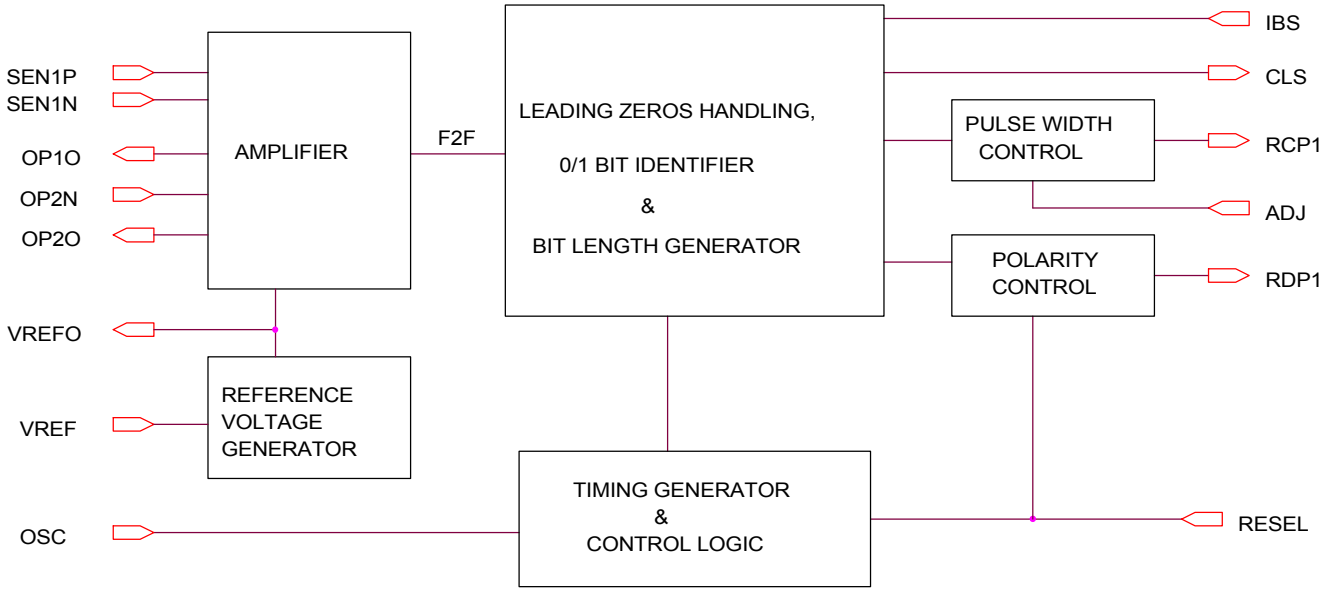
9. MAG. HEAD SIGNAL AMPLIFIER



10. BLOCK DIAGRAM



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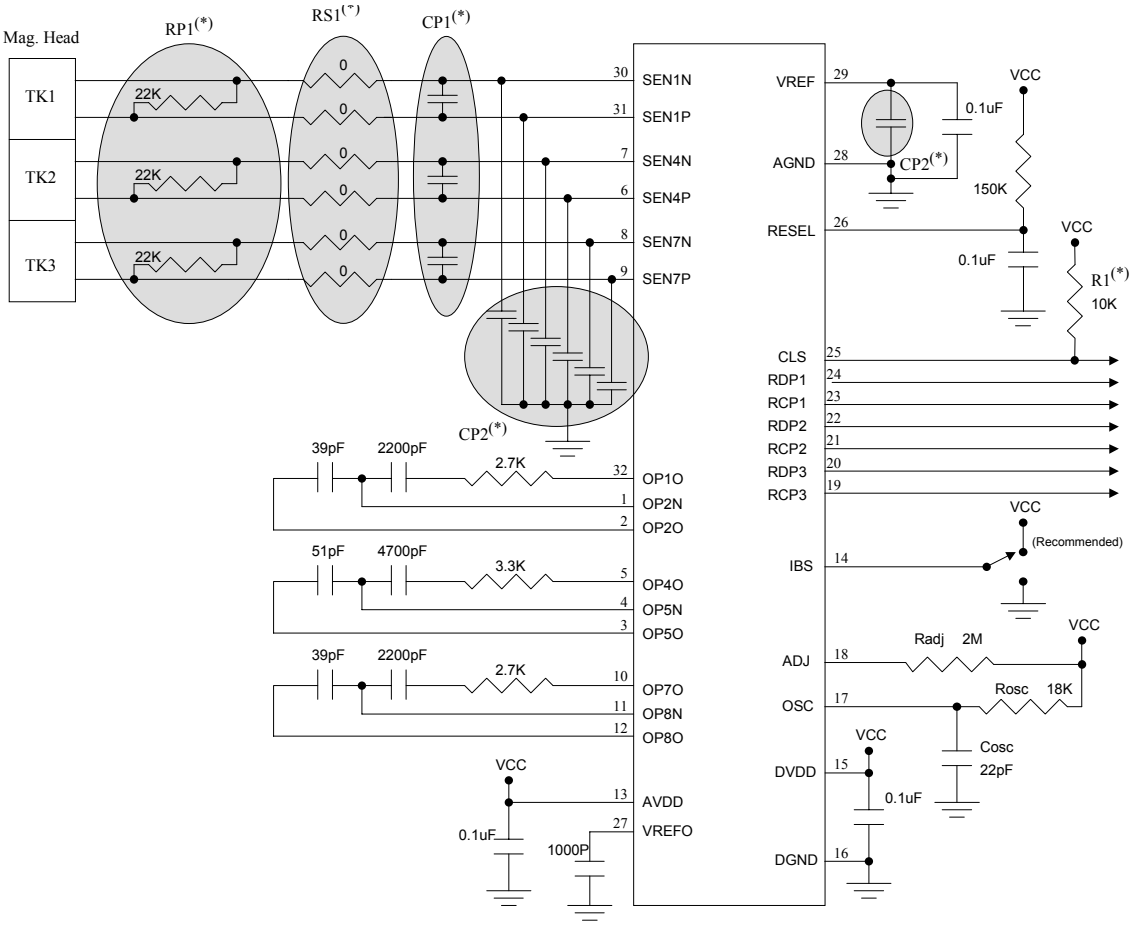
11. APPLICATION CIRCUIT



Remark:

- In typical application, RP1, CP1 and CP2 are not required.
- If necessary, add RP1 and small capacitors (CP1 and CP2) for high ESD/RS noise immunity. If CP2 capacitors are added, place them as close to MRD531B-LQ chip as possible. The typical value for CP1 and CP2 is 100pF.
- R1 is an option for 5V operation, but a must for 3.3V operation.
- If RS1 resistors are needed, keep their resistance as low as possible. Never put them with resistors higher than 500 ohm.

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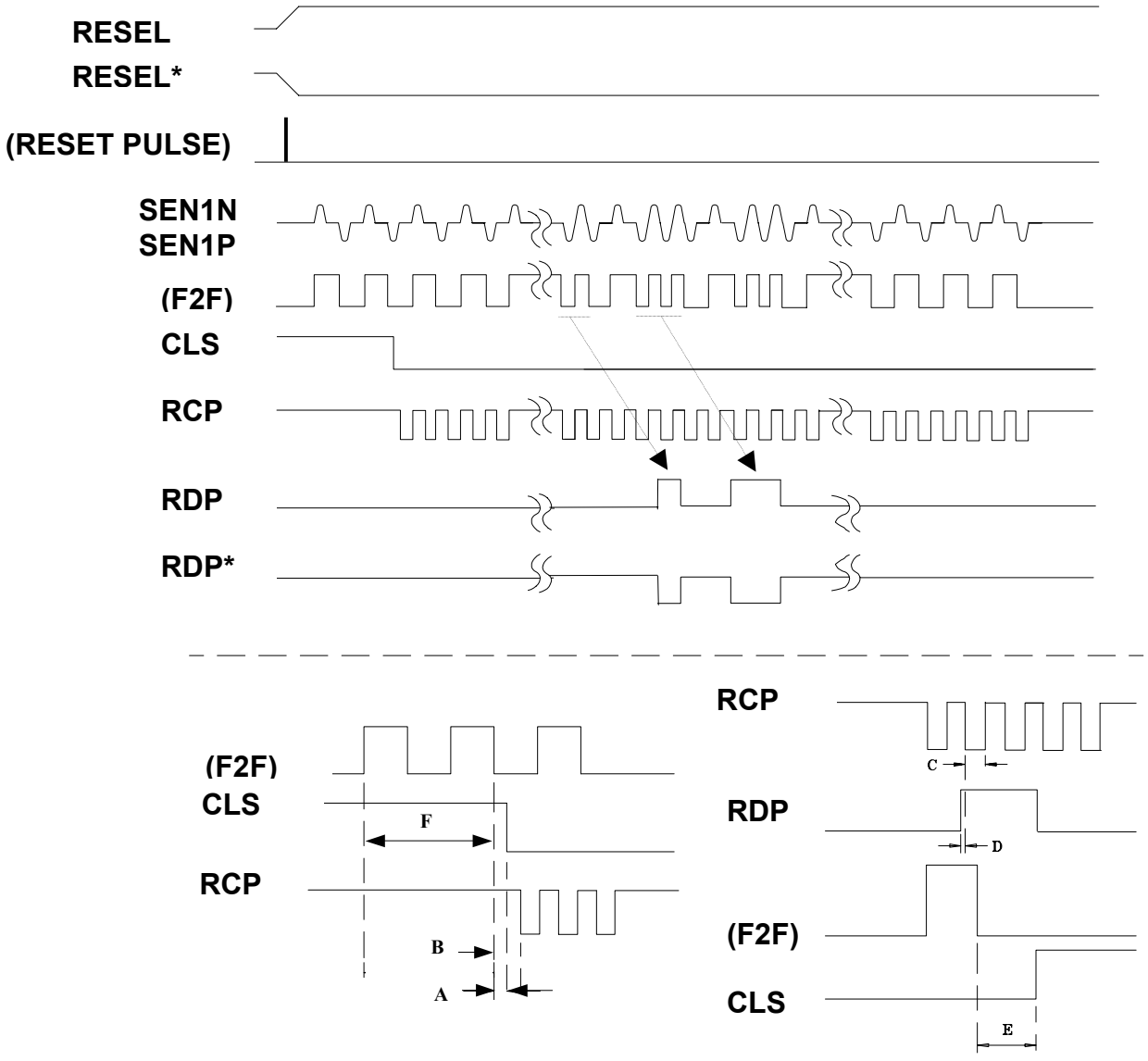
12. TIMING DIAGRAM



Time width of the A, B, C, D, E, F:

- **A: 4~8 FOSC clocks, approximate 1~2uS if FOSC=4MHz.**
- **B: 9.5~13.5 FOSC clocks; If IBS=0, the 1st RCP occurs at the 9th or 10th F2F signal reversal, dependent on data 0 or 1 starting at the 8th F2F signal reversal. If IBS=1, the 1st RCP occurs at the 12th or 13th F2F signal reversal, dependent on data 0 or 1 starting at the 11th F2F signal reversal.**
- **C: Adjustable from 7uS ~ 68uS, dependent on the frequency of FOSC and the value of Radj (an external resistor connected between VDD and ADJ); the maximum duration won't exceed 272 clocks of FOSC.**
- **D: 7 FOSC clocks, approximate 1.75uS**
- **E: 30720 clocks of FOSC, approximate 7.68mS if FOSC=4MHz.**
- **F: CLS goes Low after the 9th or 12th F2F signal reversal, dependent on IBS being set to 0 or 1 respectively**

Remark:

1. **The signal name marked with star (*) is for the condition that RESEL stays at LOW.**
2. **The signal name in parentheses means the signal inside MRD531B-LQ.**
3. **The time delay from F2F to RDP is 3 data bits (i.e. 3 RCP pulses) or 5 data bits (i.e. 5 RCP pulses), dependent on IBS being set to 0 or 1, respectively.**

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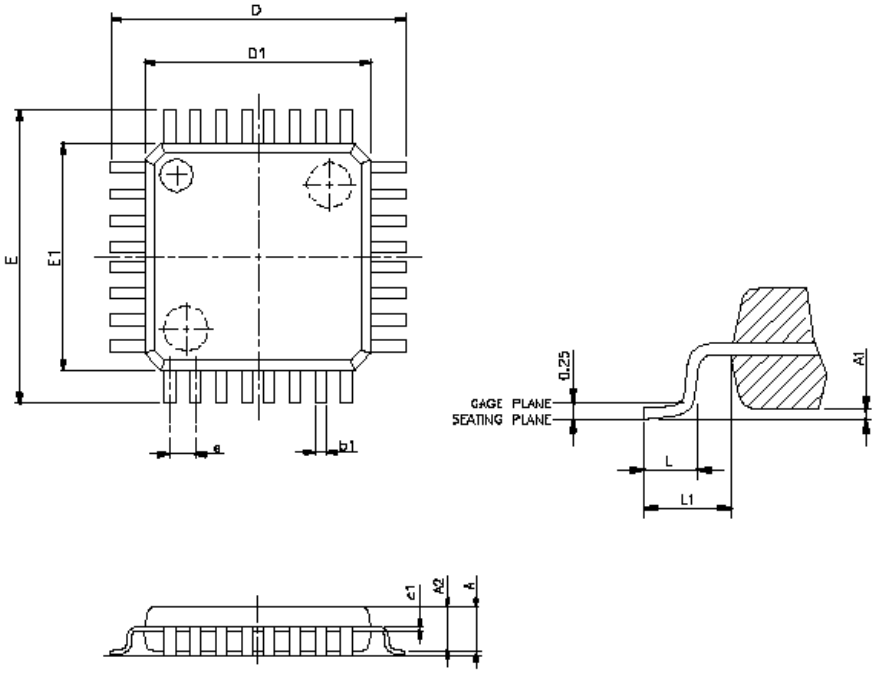
13. OUTLINE DIMENSION



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
E	9.00 BSC	
E1	7.00 BSC	
e	0.8 BSC	
b	0.30	0.45
L	0.45	0.75
L1	1 REF	

NOTES:

1. JEDEC OUTLINE: MS-026 BBA
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THE 0.08mm.